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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/663,485	09/15/2003	Takashi Kumamoto	109263-131564	2427

25943 7590 06/03/2004

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EXAMINER	
VU, QUANG D	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 06/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

AT

Office Action Summary	Application No.	Applicant(s)	
	10/663,485	KUMAMOTO, TAKASHI	
	Examiner	Art Unit	
	Quang D Vu	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-27 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-27 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-3, 8, 9, 21 and 26 are rejected under 35 U.S.C. 102(e) as being anticipated by US Patent Application Publication No. 2001/0054758 to Isaak.

Regarding claim 1, Isaak (figures 1-8) teaches a microelectronic package array, comprising:

a first microelectronic package (12) including a first carrier substrate having a first die side (16) and a first non-die side (18), a first die (70) electrically coupled to the first die side (16), and a land pad (26, 30) on the first die side (16);

a second microelectronic package (12) comprising a second carrier substrate having a second die side (16) and a second non-die side (18), a second die (70) electrically coupled to the second die side (16), and a bond pad (top portion of 26, 30) on the second non-die side (18); and

an intermediate substrate (34) having a first side (an upper surface of the substrate [34]) and a second side (a bottom surface of the substrate [34]), the first side (an upper surface of the substrate [34]) being coupled to the first die side (16) of the first carrier substrate and the second

side (a bottom surface of the substrate [34]) being coupled to the second non-die side (18) of the second carrier substrate.

Regarding claim 2, Isaak teaches the intermediate substrate further comprises:

a substantially solid core (a portion of the intermediate substrate [34]) having a first side (an upper surface of the substrate [34]) and a second side (a bottom surface of the substrate [34]);

an adhesive material (a portion of the layer [49]) disposed on the first side (an upper surface of the substrate [34]) and second side (a bottom surface of the substrate [34]) of the core; and

a conductive riser (32) disposed within the solid core (a portion of the intermediate substrate [34]).

Regarding claim 3, Isaak teaches the intermediate substrate (34) is mechanically bonded to the first die side (16) of the first carrier substrate and the second non-die side (18) of the second carrier substrate by the adhesive material (a portion of the layer [49]).

Regarding claim 8, Isaak teaches the conductive riser (32) is electrically coupled to the land pad (26, 30) of the first microelectronic package and the bond pad (top portion of 26, 30) of the second microelectronic package.

Regarding claim 9, Isaak teaches the conductive riser (32) includes a first end (an upper portion of 32) and a second end (a lower portion of 32) having conductive plating (a portion of layer 49) disposed thereon, the first (an upper portion of 32) and second (a lower portion of 32) ends being electrically bonded to the land pad (26, 30) and the bond pad (top portion of 26, 30) respectively by the conductive plating (a portion of layer 49).

Regarding claim 21, Isaak (figures 1-8) teaches a method for fabricating a microelectronic package array, comprising:

providing a first microelectronic package (12) having a first carrier substrate with a first die side (16) and a first non-die side (18), and a plurality of land pads (26, 30) disposed on the first die side (16);

providing a second microelectronic package (12) having a second carrier substrate with a second die side (16) and a second non-die side (18), and a plurality of bond pads (top portion of 26, 30) disposed on the second non-die side (18);

placing an intermediate substrate (34) having a plurality of conductive risers (32) disposed therein on the first die side (16) of a the first carrier substrate;

placing the second carrier substrate on the intermediate substrate (34) with the second non-die side (18) coming in contact with the intermediate substrate (34);

mechanically coupling the intermediate substrate (34) to the first and second carrier substrates; and

electrically coupling the plurality of conductive risers (32) with the plurality of land (26, 30) and bond pads (top portion of 26, 30).

Regarding claim 26, Isaak teaches the intermediate substrate (34) further includes a core having a first side (an upper surface of 34) and a second side (a bottom surface of 34), and an adhesive material (a portion of layer 49) disposed on the first side (an upper surface of 34) and the second side (a bottom surface of 34).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent Application Publication No. 2001/0054758 to Isaak in view of US Patent No. 5,591,353 to Davignon et al.

Regarding claim 4, Isaak differs from the claimed invention by not showing the adhesive material is a B-stage polymer. However, Davignon et al. teach the adhesive material is a B-stage (column 2, lines 13-15). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Davignon et al. into the device taught by Isaak because it is desirable securely to hold the substrate in place.

5. Claims 5-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent Application Publication No. 2001/0054758 to Isaak in view of US Patent No. 4,327,143 to Alvino et al.

Regarding claim 5, Isaak differs from the claimed invention by not showing the core is a C-stage resin. However, Alvino et al. teach the core is a C-stage resin (column 12, lines 36-40). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Alvino et al. into the device taught by Isaak because it is desirable to hold the chip in place.

Regarding claim 6, the combined device shows the C-stage resin is reinforced with a matrix to increase stiffness and control the coefficient of thermal expansion of the intermediate substrate.

6. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Isaak in view of Alvino et al., and further in view of US Patent No. 5,952,440 to Walisser et al.

Regarding claim 7, the disclosures of Isaak and Alvino et al. are discussed as applied to claims 5-6 above.

The combined device differs from the claimed invention by not showing the matrix is fiberglass cloth. However, Walisser et al. teach the matrix is fiberglass (column 10, lines 42-47). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Walisser et al. into the device taught by Isaak and Alvino et al. because it is desirable to hold chip in place.

7. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent Application Publication No. 2001/0054758 to Isaak.

Regarding claim 10, Isaak teaches the conductive plating is gold plated nickel solder. Isaak differs from the claimed invention by not showing conductive plating is tin. It would have been obvious to one having ordinary skill in the art at the time the invention was made for conductive plating is tin, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use. In re Leshin, 125 USPQ 416.

8. Claims 11-13, 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent Application Publication No. 2001/0054758 to Isaak in view of US Patent No. 6,054,337 to Solberg.

Regarding claim 11, Isaak (figures 1-8) teaches a system, comprising:

a system board (a bottom substrate);

a memory (Isaak teaches a memory chip) configured to store data, the memory disposed on the system board;

a microelectronic package array (10) disposed on the system board (a bottom substrate), the microelectronic package array comprising:

a first microelectronic package (12) including a first carrier substrate having a first die side (16) and a first non-die side (18), a first die (70) electrically coupled to the first die side (16), and a land pad (26, 30) on the first die side (16);

a second microelectronic package (12) comprising a second carrier substrate having a second die side (16) and a second non-die side (18), a second die (70) electrically coupled to the second die side (16), and a bond pad (top portion of 26, 30) on the second non-die side (18); and

an intermediate substrate (34) coupled to the first die side (16) of the first carrier substrate and the second non-die side (18) of the second carrier substrate.

Isaak differs from the claimed invention by not showing a bus disposed on the system board to facilitate data exchange; a memory configured to store data, the memory disposed on the system board and coupled to the bus; and a microelectronic package array disposed on the system board and coupled to the bus. However, Solberg teaches the memory chips, which are

connected to the data bus (column 2, lines 55-58). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Solberg into the device taught by Isaak because it provides interconnect between the chip and the external device. The combined device shows a bus disposed on the system board to facilitate data exchange; a memory configured to store data, the memory disposed on the system board and coupled to the bus; and a microelectronic package array disposed on the system board and coupled to the bus.

Regarding claim 12, Isaak teaches the intermediate substrate further comprises:

a substantially solid core (a portion of the intermediate substrate [34]) having a first side (an upper surface of the substrate [34]) and a second side (a bottom surface of the substrate [34]);

an adhesive material (a portion of the layer [49]) disposed on the first side (an upper surface of the substrate [34]) and second side (a bottom surface of the substrate [34]) of the core; and

a conductive riser (32) disposed within the solid core (a portion of the intermediate substrate [34]).

Regarding claim 13, Isaak teaches the intermediate substrate (34) is mechanically bonded to the first die side (16) of the first carrier substrate and the second non-die side (18) of the second carrier substrate by the adhesive material (a portion of the layer [49]).

Regarding claim 18, Isaak teaches the conductive riser (32) is electrically coupled to the land pad (26, 30) of the first microelectronic package and the bond pad (top portion of 26, 30) of the second microelectronic package.

Regarding claim 19, Isaak teaches the conductive riser (32) includes a first end (an upper portion of 32) and a second end (a lower portion of 32) having conductive plating (a portion of layer 49) disposed thereon, the first (an upper portion of 32) and second (a lower portion of 32) ends being electrically bonded to the land pad (26, 30) and the bond pad (top portion of 26, 30) respectively by the conductive plating (a portion of layer 49).

9. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Isaak in view of Solberg, and further in view of US Patent No. 5,591,353 to Davignon et al.

Regarding claim 14, the disclosures of Isaak and Solberg are discussed as applied to claims 11-13 above.

Isaak and Solberg differ from the claimed invention by not showing the adhesive material is a B-stage polymer. However, Davignon et al. teach the adhesive material is a B-stage (column 2, lines 13-15). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Davignon et al. into the device taught by Isaak and Solberg because it is desirable securely to hold the substrate in place.

10. Claims 15-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Isaak in view of Solberg, and further in view of US Patent No. 4,327,143 to Alvino et al.

The disclosures of Isaak and Solberg are discussed as applied to claims 11-13 above.

Regarding claim 15, Isaak and Solberg differ from the claimed invention by not showing the core is a C-stage resin. However, Alvino et al. teach the core is a C-stage resin (column 12, lines 36-40). Therefore, it would have been obvious to one having ordinary skill in the art at the

time the invention was made to incorporate the teaching of Alvino et al. into the device taught by Isaak and Solberg because it is desirable to hold the chip in place.

Regarding claim 16, the combined device shows the C-stage resin is reinforced with a matrix to increase stiffness and control the coefficient of thermal expansion of the intermediate substrate.

11. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Isaak and Solberg in view of Alvino et al., and further in view of US Patent No. 5,952,440 to Walisser et al.

Regarding claim 17, the disclosure of Isaak, Solberg and Alvino et al. are discussed as applied to claims 15-16 above.

The combined device differs from the claimed invention by not showing the matrix is fiberglass cloth. However, Walisser et al. teach the matrix is fiberglass (column 10, lines 42-47). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Walisser et al. into the device taught by Isaak, Solberg and Alvino et al. because it is desirable to hold chip in place.

12. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Isaak and Solberg.

Regarding claim 20, the combined device teaches the conductive plating is gold plated nickel solder (Isaak). Isaak and Solberg differ from the claimed invention by not showing conductive plating is tin. It would have been obvious to one having ordinary skill in the art at the time the invention was made for conductive plating is tin, since it has been held to be within the

general skill of a worker in the art to select a known material on the basis of its suitability for the intended use. In re Leshin, 125 USPQ 416.

13. Claims 22-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent Application Publication No. 2001/0054758 to Isaak in view of US Patent No. 5,145,303 to Clarke.

Regarding claim 22, Isaak differs from the claimed invention by not showing placing the microelectronic package array in a vacuum chamber; creating a vacuum in the vacuum chamber; applying heat to the microelectronic package array; applying pressure to the microelectronic package array; releasing the pressure; and cooling the microelectronic package array. However, Clarke teaches the microelectronic package in chamber (column 1, lines 15-19). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Clarke into the device taught by Isaak because it eliminates the contamination. The combined device shows placing the microelectronic package array in a vacuum chamber; creating a vacuum in the vacuum chamber; applying heat to the microelectronic package array; applying pressure to the microelectronic package array; releasing the pressure; and cooling the microelectronic package array.

Regarding claim 23, the combined device differs from the claimed invention by not showing creating a vacuum comprises establishing a pressure of about less than 10 kilo Pascals. It would have been obvious to one having ordinary skill in the art at the time the invention was made for creating a vacuum comprises establishing a pressure of about less than 10 kilo Pascals because it eliminates the contamination. Furthermore, it has been held that discovering an

optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Regarding claim 24, the combined device differs from the claimed invention by not showing applying heat comprises raising the temperature to about between 150^0C and 350^0C. It would have been obvious to one having ordinary skill in the art at the time the invention was made for applying heat comprises raising the temperature to about between 150^0C and 350^0C because it eliminates the contamination. Furthermore, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding claim 25, the combined device differs from the claimed invention by not showing applying a pressure comprises increasing the pressure to a range between 0.5 mega Pascals and 10 mega Pascals. It would have been obvious to one having ordinary skill in the art at the time the invention was made for applying a pressure comprises increasing the pressure to a range between 0.5 mega Pascals and 10 mega Pascals because it eliminates the contamination. Furthermore, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

14. Claim 27 is rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent Application Publication No. 2001/0054758 to Isaak in view of US Patent No. 5,591,353 to Davignon et al. and US Patent No. 4,327,143 to Alvino et al.

Regarding claim 27, Isaak differs from the claimed invention by not showing the adhesive material is a B-stage polymer. However, Davignon et al. teach the adhesive material is a B-stage (column 2, lines 13-15). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Davignon et al. into the device taught by Isaak because it is desirable securely to hold the substrate in place.

Isaak and Davignon et al. further differ from the claimed invention by not showing the core is a C-stage resin. However, Alvino et al. teach the core is a C-stage resin (column 12, lines 36-40). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Alvino et al. into the device taught by Isaak and Davignon et al. because it is desirable to hold the chip in place.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quang D Vu whose telephone number is 571-272-1667. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

qv
May 28, 2004.

Sara Crane
Primary Examiner